REMARKS/ARGUMENTS

Claims 1-39 are pending in the application. Claims 1, 2, 6, 11-12, 14, 15, 19, 24-25, 27, 28, 32, and 37-38 have been amended. Reconsideration is respectfully requested. Applicants submit that the pending claims 1-39 are patentable over the art of record and allowance is respectfully requested of claims 1-39.

Applicants would like to thank Examiner Misiura for holding a telephone interview with their representative, Janaki K. Davda, on March 13, 2006, at 2:30 p.m. (EST). Proposed claim amendments to claims 1, 2, and 6 and the cited prior art were discussed. In particular, Applicants' representative pointed to Applicants' Specification on page 1, paragraph 2, page 5, paragraph 19, and page 7, paragraphs 27-28, and submitted that the claimed invention is directed to the interaction of an I/O device and an I/O device driver that use an event data structure to communicate, so that the I/O device driver avoids I/O reads and writes across a bus connecting a host system to an I/O device (Applicants' Specification, page 1, paragraph 2). Applicants' representative also pointed out that the event data structure has, for example, armed and unarmed states, which are distinct from the full state of a transfer queue unit as described in the Kobayakawa patent. No agreement was reached.

The Specification was objected to. Applicants have amended the Specification to correct a minor error by changing "FIG. 2A" to "FIG. 2" and to overcome the objection.

Claims 1-7, 9, 11, 12, 14-20, 22, 24, 25, 27-33, 35, 37, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayakawa et al. (U.S. Patent No. 5,557,744). Applicants respectfully traverse.

Anticipation requires that the identical invention must be shown in a single reference in as complete detail as is contained in the claims. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully submit that the Kobayakawa patent does not teach the identical invention claimed by Applicants.

As described in Applicants' Specification, page 1, paragraph 2, upon an interrupt from an I/O device, an I/O device driver executing at a host system runs an Interrupt Service Routine

(ISR) that checks the state of an I/O device interrupt for each I/O device, one at a time. Then, if a particular I/O device generated the interrupt, the ISR disables interrupts so that the same I/O device cannot generate another interrupt, acknowledges the interrupt, processes the interrupt, and enables interrupts so that the I/O device can generate another interrupt. Typically, an I/O device has registers for interrupt status/cause, masking, and acknowledgement. Thus, the ISR performs an I/O read of the register across a bus for interrupt status/cause to determine whether a particular I/O device generated the interrupt and to determine the type of interrupt. The ISR performs I/O writes across the bus to the register for masking to disable and enable the interrupts. Additionally, the ISR performs an I/O write across the bus to the register for acknowledgement to acknowledge the interrupt. I/O reads and I/O writes go across the bus connecting the I/O device to the host system. Such I/O reads and I/O writes across the bus for interrupt processing may degrade system performance and result in interrupt processing latency and system overhead. Also, the I/O reads and I/O writes may be Memory Mapped I/O (MMIO) reads/writes.

To avoid such I/O reads and I/O writes across the bus, claim 1 describes a method for interrupt processing in which it is determined that an event has occurred. A state of an event data structure is determined, wherein the event data structure includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device (e.g., Applicants' Specification, page 5, paragraph 19). Then, an event entry is written into the event data structure in response to determining that the event has occurred and based on the state of the event data structure (e.g., Applicants' Specification, page 7, paragraphs 27-28).

The Kobayakawa patent addresses a different problem. In particular, the Kobayakawa patent describes a multiprocessor system in which each processor has a transmission unit and a reception unit for communication between processors (Col. 1, lines 19-21) and suggests that a suitable management system using an operating system and a data processing program has not yet been realized (Col. 1, lines 28-30). The Kobayakawa patent describes that the object of its invention is to provide a multiprocessor system enabling a certain communication process between processors by using an operating system or a data processing program (Col. 1, lines 33-38).

In particular, the Kobayakawa patent describes a first register for storing information

indicating whether a transfer queue unit is full (Abstract). When a decision unit determines that the first register indicates a full state, a save unit saves a transfer request to a save area and an issuing unit issues an interruption request to an interruption processing unit (Col. 4, lines 56-63). The interruption processing unit supervises the contents of the read pointer and the write pointer to detect a vacant area for the transfer request in the transfer queue unit and issues an enqueuing request to the enqueuing unit when the transfer queue unit has a vacant area (Col. 6, lines 1-10). The enqueuing unit enqueues the transfer request, which is saved in the save area, into the transfer queue unit (Col. 6, lines 1-10).

The transfer queue unit of the Kobayakawa patent does not anticipate the claimed event data structure that includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device. Therefore, Applicants respectfully submit that claim 1 is not anticipated by the Kobayakawa patent.

Claims 14 and 27 are not anticipated by the Kobayakawa patent for at least the same reasons as were discussed with respect to claim 1. Furthermore, claims 14 and 27 describe an Input/Output device that is operable to perform the claimed elements. The Kobayakawa patent describes a network and processors (FIG. 3), but these do not anticipate that an I/O device performs the claimed elements.

Dependent claims 2-5, 15-18, and 28-31 incorporate the language of independent claims 1, 14, and 27 and add additional novel elements. Therefore, dependent claims 2-5, 15-18, and 28-31 are not anticipated by the Kobayakawa patent for at least the same reasons as were discussed with respect to claims 1, 14, and 27.

Additionally, dependent claims 2, 15, and 28 describe issuing an interrupt in response to determining that the state of the event data structure is armed and that a condition exists to cause an interrupt, wherein events are posted to the event data structure when the state of the event data structure is one of armed and unarmed and wherein interrupts are not issued when the state of the event data structure is unarmed (e.g., Applicants' Specification, page 5, paragraph 20; page 7, paragraphs 27-28; FIG. 3). The Kobayakawa patent describes that the transfer queue unit has a full state and that the indication of the full state is reset when the full state of the transfer queue is released after the data transfer is completed in the transmission unit (Col. 4, lines 57-63; Col. 5, lines 30-35; FIG. 2). Such a transfer queue unit and a full state do not anticipate issuing an

interrupt in response to determining that the state of the event data structure is armed and that a condition exists to cause an interrupt, wherein events are posted to the event data structure when the state of the event data structure is one of armed and unarmed and wherein interrupts are not issued when the state of the event data structure is unarmed.

Claim 6 describes a method for interrupt processing in which it is determined that an interrupt has occurred. An event entry in an event data structure is read in response to determining that the interrupt has occurred, wherein the event data structure includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device (e.g., Applicants' Specification, page 5, paragraph 19). A state of a structure state indicator is updated to unarmed to indicate that interrupts are not allowed (e.g., Applicants' Specification, page 7, paragraphs 27-28).

The transfer queue unit of the Kobayakawa patent does not anticipate the claimed event data structure that includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device. Also, when an interrupt is received in the Kobayakawa patent, the transfer queue unit is not read. Instead, the Kobayakawa enqueues a transfer request when an interrupt is issued. This does not anticipate, and, teaches away from, reading an event entry in response to determining that an interrupt has occurred (Col. 6, lines 1-10). Moreover, the full state of the Kobayakawa transfer queue unit does not anticipate the clamed unarmed state in which interrupts are not allowed.

Claims 19 and 32 are not anticipated by the Kobayakawa patent for at least the same reasons as were discussed with respect to claim 6. Furthermore, claims 19 and 32 describe an Input/Output device driver that is operable to perform the claimed elements. The Kobayakawa patent does not teach that an I/O device driver performs such elements.

Dependent claims 7, 9, 11, 12, 20, 22, 24, 25, 33, 35, 37, and 38 incorporate the language of independent claims 6, 19, and 32 and add additional novel elements. Therefore, dependent claims 7, 9, 11, 12, 20, 22, 24, 25, 33, 35, 37, and 38 are not anticipated by the Kobayakawa patent for at least the same reasons as were discussed with respect to claims 6, 19, and 32.

Claims 8, 21, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayakawa et al. (U.S. Patent No. 5,557,744). Applicants respectfully traverse.

The Kobayakawa patent does not teach or suggest the subject matter of claims 6, 19, and 32. For example, the Kobayakawa patent does not teach or suggest determining that an interrupt has occurred, reading an event entry in an event data structure in response to determining that the interrupt has occurred, wherein the event data structure includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device, and updating a state of a structure state indicator to unarmed to indicate that interrupts are not allowed.

Claims 8, 21, and 34 describe determining whether to allow interrupts, updating the state in a structure state indicator to armed in response to determining that interrupts are to be allowed, and waiting for an interrupt. Claims 8, 21, and 34 incorporate the language of independent claims 6, 19, and 32 and add additional novel elements. Therefore, dependent claims 8, 21, and 34 are not taught or suggested by the Kobayakawa patent for at least the same reasons as were discussed with respect to claims 6, 19, and 32.

Claims 10, 23, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayakawa et al. (U.S. Patent No. 5,557,744) in view of Yamaoka (U.S. Patent No. 5,214,759). Applicants respectfully traverse.

The Kobayakawa patent does not teach or suggest the subject matter of claims 6, 19, and 32. There is no motivation to combine the Kobayakawa and Yamaoka patents, but, even if combined, the combination does not teach or suggest the claimed subject matter. For example, the Yamaoka patent does not cure the defects of the Kobayakawa patent as the Yamaoka patent does not teach or suggest determining that an interrupt has occurred, reading an event entry in an event data structure in response to determining that the interrupt has occurred, wherein the event data structure includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device, and updating a state of a structure state indicator to unarmed to indicate that interrupts are not allowed.

Claims 10, 23, and 32 incorporate the language of independent claims 6, 19, and 32 and add additional novel elements. Therefore, dependent claims 10, 23, and 32 are not taught or

suggested by the Kobayakawa patent or the Yamaoka patent, either alone or in combination, for at least the same reasons as were discussed with respect to claims 6, 19, and 32.

Also, claims 10, 23, 36 describe initializing the event data structure, notifying an I/O device of the location of the event data structure, and updating the state of the structure state indicator to unarmed. The Yamaoka patent describes a communication buffer used for communication between OS's (Col. 5, lines 2-10), which does not teach or suggest the use of the claimed event data structure by an I/O device driver and an I/O device (e.g., claims 19 and 32).

Claims 13, 26, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayakawa et al. (U.S. Patent No. 5,557,744) in view of Schmidt (U.S. Patent No. 6,792,483). Applicants respectfully traverse.

The Kobayakawa patent does not teach or suggest the subject matter of claims 6, 19, and 32. There is no motivation to combine the Kobayakawa and Schmidt patents, but, even if combined, the combination does not teach or suggest the claimed subject matter. For example, the Schmidt patent does not cure the defects of the Kobayakawa patent as the Schmidt patent does not teach or suggest determining that an interrupt has occurred, reading an event entry in an event data structure in response to determining that the interrupt has occurred, wherein the event data structure includes one or more entries, and wherein each of the entries is capable of storing event specific parameters and an event code field that identifies at least one of an event source and function of an I/O device, and updating a state of a structure state indicator to unarmed to indicate that interrupts are not allowed.

Claims 13, 26, and 39 incorporate the language of independent claims 6, 19, and 32 and add additional novel elements. Therefore, dependent claims 13, 26, and 39are not taught or suggested by the Kobayakawa patent or the Yamaoka patent, either alone or in combination, for at least the same reasons as were discussed with respect to claims 6, 19, and 32.

Also, claims 13, 26, and 39 describe generating multiple event data structures for one I/O device, wherein events for different I/O device functions are associated with one of the multiple event data structures, and dynamically mapping each of the multiple event data structures to a processor. The Schmidt patent describes that each device driver has a send queue and a receive or target queue, where the send queue is used for sending data from a server and the receive queue is used for receiving data from the server (Col. 5, lines 12-23). The device drivers, rather

than driving I/O devices, drive data exchanges between the LPAR partitions (Col. 5, lines 14-16). Thus, the Schmidt patent teaches away from generating multiple event data structures for one I/O device, wherein events for different I/O device functions are associated with one of the multiple event data structures, and dynamically mapping each of the multiple event data structures to a processor.

Conclusion

For all the above reasons, Applicants submit that the pending claims 1-39 are patentable over the art of record. Applicants have not added any claims. Nonetheless, should any additional fees be required, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact her at (310) 553-7973 if the Examiner believes such contact would advance the prosecution of the case.

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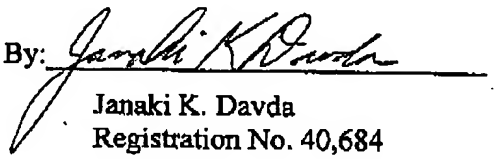
By: 

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